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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,127	04/05/2001	Chaojun Deng	43774/209425	4908
20350 7590 12/28/2007 TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			EXAMINER MURPHY, RHONDA L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/827,127

Applicant(s)

DENG, CHAOJUN

Examiner

Rhonda Murphy

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 69-74 and 78-96 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 69-74 and 78-96 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This communication is responsive to the amendment filed on 9/24/07.
Accordingly, claims 1-68 and 75-77 have been canceled, claims 79-96 added and claims 69-74 and 78-96 are currently pending in this application.

Response to Arguments

1. Applicant's arguments with respect to claims 69-74 and 78-96 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

1. Claim 94 is objected to because of the following informality:
2. Examiner is questioning whether applicant intended to use the term "base card", instead of "base board" in line 2 of claim 94.
3. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 69 – 73 and 78 - 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kastenholz et al. (US 2006/0007946 A1).

Regarding claim 69, Kastenholz teaches a system for data communication, the system comprising:

a first circuit card (Figs. 2 and 3; line card module 102) including one or more first interfaces (page 4, paragraph 45; I/O interfaces) and one or more first logic components for processing control (page 4, paragraph 45);

a first transfer card (Fig. 3; local line card 202) coupled to the first circuit card (see Fig. 3; page 5, paragraph 50) through at least a first base card (Fig. 3; page 5, paragraph 50; printed circuit board), the first base card being coupled directly to the first transfer card (see Fig. 3; page 5, paragraph 50);

a second circuit card (Figs 2 and 5; expanded interconnect board 138) including one or more second interfaces (Fig. 5; ports) and one or more second logic components for processing control (page 8, paragraph 74);

a second transfer card (Fig. 5; ASIC 410 a/b) coupled to the second circuit card (see Fig. 5) through at least a second base card (Fig. 5, page 4, paragraph 44; printed circuit board), the second base card being coupled directly to the second transfer card (see Fig. 5);

a first switched network card (Figs. 2, 3 and 5; local interconnect module 118) to at least perform an exchange function between the first circuit card and the second circuit card (Fig. 2; via communication lines between 102, 118 and 138), the first switched network card (118) and the first circuit card (102) being different types of

cards (page 5, paragraphs 50-51; 102 is a line card and 118 is a module divided into planes, containing an ASIC);

a first interface card (Fig. 3; interconnect board 218) coupled to the first switched network card (see Fig. 3; page 5, paragraph 51) through at least a third base card (Fig. 3; page 5, paragraph 51; printed circuit board), the third base card being coupled directly to the first interface card (see Fig. 3);

a second interface card (Fig. 3, interconnect board 220) coupled to the first switched network card (see Fig. 3; page 5, paragraph 51);

a first data communication link (Fig. 3, communication lines 217) connecting the first transfer card and the first interface card (page 5, paragraph 50);

a second data communication link (Fig. 5, communication lines between 220 and 138) connecting the second transfer card and the second interface card (see Fig. 5);

wherein: the first transfer card, and the first circuit card are associated with a first framework (Fig. 2; page 8, paragraph 70; chassis 101); the first interface card, the second interface card, and the first switched network card, are associated with a second framework (Figs. 2 and 3, page 8, paragraph 70; chassis 103), the first framework and the second framework being associated with different physical locations (Fig. 2; page 8, paragraph 70; chassis 101 and 103 in different physical locations).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes (in each framework, in different physical locations - chassis 101 and 103), in order to provide a means for connecting the cards.

Although Kastenholz teaches base cards, transfer cards and circuit cards, Kastenholz fails to explicitly disclose the cards not being a part of one another.

However, it would have been obvious to one skilled in the art to separate elements, in order to have distinct elements within a system.

Regarding claim 70, Kastenholz teaches each of the first data communication link and the second data communication link including an optical fiber (page 5, paragraph 50: SONET I/O ports; page 8, paragraph 73: Gigabit Ethernet interfaces, inherently include optical fibers).

Regarding claim 71, Kastenholz teaches the first backplane and the second backplane are the same; the first base card and the second base cards are the same.

Regarding claim 72, Kastenholz teaches a system for data communication, the system comprising:

- a first circuit card (Figs. 2 and 3; line card module 102) including one or more first interfaces (page 4, paragraph 45; I/O interfaces) and one or more first logic components for processing control (page 4, paragraph 45);

- a first transfer card (Fig. 3; local line card 202) coupled to the first circuit card (see Fig. 3; page 5, paragraph 50);

- a second circuit card (Figs. 2 and 3; line card module 104; although line module 102 is illustrated in Figure 3, line card module 104 is identical to 102; page 4, paragraph

44) including one or more second interfaces (page 4, paragraph 45; I/O interfaces) and one or more second logic components for processing control (page 4, paragraph 45);

a second transfer card (Fig. 3; local line card 202) coupled to the second circuit card (see Fig. 3; page 5, paragraph 50);

a first switched network card (Figs. 2, 3 and 5; local interconnect module 118) to at least perform an exchange function between the first circuit card and the second circuit card (Fig. 2; via communication lines between 102/104 and 118), the first switched network card (118) and the first circuit card (102) being different types of cards (page 5, paragraphs 50-51; 102 is a line card and 118 is a module divided into planes, containing an ASIC);

a first interface card (Fig. 3; interconnect board 218) coupled to the first switched network card (see Fig. 3; page 5, paragraph 51);

a second interface card (Fig. 3, interconnect board 220) coupled to the first switched network card (see Fig. 3; page 5, paragraph 51);

a first data communication link (Fig. 3, communication lines 217) connecting the first transfer card and the first interface card (page 5, paragraph 50);

a second data communication link (Fig. 3, communication lines 217 – of line card module 104) connecting the second transfer card and the second interface card (see Fig. 5);

wherein: the first transfer card and the first circuit card are associated with a first framework (Fig. 2; page 8, paragraph 70; chassis 101); the first interface card, the second interface card and the first switched network card are

associated with a second framework (Figs. 2 and 3, page 8, paragraph 70; chassis 103), the first framework and the second framework being associated with different physical locations (Fig. 2; page 8, paragraph 70; chassis 101 and 103 in different physical locations); each of the first data communication link and the second data communication link includes an optical fiber (page 5, paragraph 50: SONET I/O ports; page 8, paragraph 73: Gigabit Ethernet interfaces, inherently include optical fibers).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes (in each framework, in different physical locations - chassis 101 and 103), in order to provide a means for connecting the cards.

Although Kastenholz teaches transfer cards and circuit cards, Kastenholz fails to explicitly disclose the cards not being a part of one another.

However, it would have been obvious to one skilled in the art to separate elements, in order to have distinct elements within a system.

Note: Reference is made to line card module 104 throughout the rejection. Line card module 104 is illustrated in Figure 2 and is identical to line card module 102.

Therefore, the other figures illustrating components and connections to/from line card module 102 also applies to line card module 104 (Kastenholz page 4, paragraph 44).

Regarding claim 73, Kastenholz teaches the first switched network card not receiving any data signal that does not transmit through a circuit card (see Fig. 2; all

communication to the first switched network (interconnect module 118) goes through the circuit cards (line card module 102 and 104).

Regarding claim 78, Kastenholz teaches the system of claim 72.

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to determine a first backplane and a second backplane are the same, since the first circuit card and second circuit card are within the same chassis.

Regarding claim 79, Kastenholz teaches a smooth capacity expandable system for data communications, the system comprising:

- a circuit card (Figs. 2 and 3; line card module 102) including a processing control logic (page 4, paragraph 45), an outside interface (Fig. 3; ports 202g; page 5, paragraph 50), and a first internal interface (ports 202a-f);

- a switched network card (Figs. 2, 3 and 5; local interconnect module 118) including a second internal interface (Fig. 3; ports);

- a transfer card (Fig. 3; local line card 202) including a first optical interface (ports) connected with an internal optical fiber (page 5, paragraph 50),

- an interface card (Fig. 3; interconnect board 218) including a second optical interface (ports) connected with the internal optical fiber (page 5, paragraph 53),

wherein the first internal interface, the second internal interface, the first electrical interface, and the second electrical interface use the same interface standard (SONET, Ethernet page 5, paragraphs 50 and 53); and

wherein:

the circuit card supports a connection with the switched network card through the first internal interface and the second internal interface (via communication lines between 102 and 118).

Regarding claim 80, Kastenholz teaches the system of claim 79, further comprising:

a circuit card framework (Fig. 3; 102); and

an interface framework (118);

wherein:

the circuit card framework includes the circuit card (see Fig. 3; 102), the transfer card (see Fig. 3; 202),

the interface framework includes the switched network card (118), the interface card (218), and the transfer card and the interface card being interconnected through the internal optical fiber (communication lines between 202 and 218).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes wherein the first internal interface and the transfer card are electrically connected via the first back plane and the second internal interface and the interface card being electrically connected via the second back plane in order to provide a means for connecting the cards.

Regarding claim 81, Kastenholz teaches the system of claim 80 wherein the interface framework includes a plurality of switched network cards therein for expanding exchange capacity (Fig. 2; 118-132).

Regarding claim 82, Kastenholz teaches the system of claim 80 wherein the circuit card framework includes a plurality of circuit cards therein for expanding an ability of receiving external data (Fig. 2; 102-116).

Regarding claim 83, Kastenholz teaches the system of claim 80 wherein the number of interface cards, the number of optical fibers, and the number of circuit card frameworks connected to the optical fibers are changeable for different capacity demands (page 4, paragraph 42).

Regarding claim 84, Kastenholz teaches the system of claim 83 wherein the circuit card framework and the interface framework are at different locations (Fig. 2; chassis 101 and 103).

Regarding claim 85, Kastenholz teaches the system of claim 79 wherein the circuit card support a plurality of external protocols associated with a POS interface, an ATM interface, and/or an Giga-bit interface (page 4, paragraphs 45-46).

Regarding claim 86, Kastenholz teaches the system of claim 79 including a first internal interface and a second internal interface.

Kastenholz fails to explicitly teach the first internal interface and a second internal interface each support 8B/10B signals coding.

However, Kastenholz does disclose a Gigabit Ethernet standard. It is well known in the art that 8B/10B signal coding is used in Gigabit Ethernet implementations.

Therefore, it would have been obvious to one skilled in the art to include 8B/10B signal coding, for the purpose of encoding eight data bits into a 10 bit transmission sequence.

Regarding claim 87, Kastenholz teaches the system of claim 80 wherein a plurality of transfer cards are included in a base card (Fig. 3; page 5, paragraph 50; printed circuit board), the base card being connected to a plurality of circuit cards of the circuit card framework (Fig. 3; page 5, paragraph 50; printed circuit board).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes, in order to provide a means for connecting the cards.

Regarding claim 88, Kastenholz teaches a method for implementing smooth capacity expansion for data communications, the method comprising:

receiving an external signal by a circuit card (102; page 4, paragraph 45);

converting the external signal into an internal signal of the circuit card (page 4, paragraphs 45-46);

receiving the converted internal signal by a transfer card (page 5, paragraph 50;

converting the converted internal signal into an optical signal (page 5, paragraph 50);

transmitting the optical signal to an interface card through an optical fiber (page 5, paragraph 50-51);

transmitting the electric signal to a switched network card (page 8, paragraph 70; chassis electrically coupled);

wherein the number of transfer cards, the number of interface cards, the number of optical fibers, and the number of switched network cards can be increased with the number of circuit cards (page 4, paragraph 42).

Kastenholz fails to explicitly disclose converting the optical signal into an electric signal by the interface card.

However, Kastenholz does disclose the chassis being electrically coupled on page 8, paragraph 70.

Therefore, it would have been obvious to one skilled in the art to convert the optical signal into an electric signal, in order to provide an electrical connection between the elements.

Regarding claim 89, Kastenholz teaches the method of claim 88, the method comprising:

setting up, according to an increase of capacity, an independent circuit card framework including the circuit card, the transfer card, and a back plane therein (page 4, paragraph 42);

wherein:

an internal interface of the circuit card and the transfer card are electrically interconnected (page 5, paragraph 50; via printed circuit boards);

the process for converting the converted internal signal into an optical signal is performed by the transfer cards (page 5, paragraph 50);

the process for transmitting the optical signal to an interface card through an optical fiber includes transmitting the optical signal to a framework for the switched network cards through the optical fiber (page 5, paragraph 52-53).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes, in order to provide a means for connecting the cards.

Regarding claim 90, Kastenholz teaches the method of claim 88, and further comprising increasing the number of the switched network cards for expanding capacity.

Regarding claim 91, Kastenholz teaches the method of claim 88, and further comprising increasing the number of the circuit cards to increase the ability to receive external data (page 4, paragraph 42).

Regarding claim 92, Kastenholz teaches the method of claim 88, and further comprising:

setting up different circuit cards for supporting different protocols respectively (page 2, paragraph 15);

converting external signals corresponding to different protocols into internal signals with the same format (page 2, paragraph 17);

transmitting the internal signals to the switched network card for processing; wherein the protocols include POS interface protocol, ATM interface protocol and Gigabit interface protocol (page 4, paragraphs 45-46).

Regarding claim 93, Kastenholz teaches the method of claim 92 including a high speed internal signal.

Kastenholz fails to explicitly teach the internal signal as a high speed serial signal supporting 8B/10B signals coding.

However, Kastenholz does disclose a Gigabit Ethernet standard. It is well known in the art that 8B/10B signal coding is used in Gigabit Ethernet implementations.

Therefore, it would have been obvious to one skilled in the art to include 8B/10B signal coding, for the purpose of encoding eight data bits into a 10 bit transmission sequence.

Regarding claim 94, Kastenholz teaches the method of claim 88, and further comprising:

integrating the transfer cards into a base board (page 5, paragraph 50; printed circuit board), the base card supporting to convert the converted internal signal from the circuit card into the optical signal and to transmit the optical signal to the interface card (page 5, paragraphs 50-51);

wherein the process for transmitting the electric signal to a switched network card is performed for exchanging (page 5, paragraphs 50, 53; page 8, paragraph 70).

Regarding claim 95, Kastenholz teaches a smooth capacity expandable system of data communications, the system comprising:

a circuit card (Figs. 2 and 3; line card module 102) including a processing control logic (page 4, paragraph 45), an outside interface (Fig. 3; ports 202g; page 5, paragraph 50), and a first internal interface (ports 202a-f);

a switched network card (Figs. 2, 3 and 5; local interconnect module 118) including a second internal interface (Fig. 3; ports);

a transfer card (Fig. 3; local line card 202) including a first optical interface (ports) connected with an internal optical fiber (page 5, paragraph 50),

an interface card (Fig. 3; interconnect board 218) including a second optical interface (ports) connected with the internal optical fiber (page 5, paragraph 53), the interface card being connected with the transfer card via the internal optical fiber (see Fig. 3; communication lines between 218 and 202);

Kastenholz fails to explicitly teach a first electrical interface connected with the first internal interface and a second electrical interface connected with the switched network card.

However, Kastenholz does disclose the chassis being electrically coupled on page 8, paragraph 70.

Therefore, it would have been obvious to one skilled in the art to determine an electrical connection exists with the first internal interface and with the switched network card, in order to provide an electrical connection between these elements.

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes, in order to provide a means for connecting the cards. Furthermore, it would have been obvious for the backplanes to provide multiple interface slots for the circuit card and switched network card to be inserted into the system, since Kastenholz

teaches adding, subtracting, changing and plugging modules in the system (page 4, paragraph 42).

Regarding claim 96, Kastenholz teaches the system of claim 95 wherein the circuit card (Fig. 3; 102), and the transfer card (202), are located in an independent framework (see Fig. 3; 102);

the switched network card (118) and the interface card (218) are located in another independent framework (see Fig. 3; 118);

the transfer card and the interface card are interconnected by the internal optical fiber (communication lines between 202 and 218);

the numbers of circuit cards and the number of switched network cards are increasable (page 4, paragraph 42).

Kastenholz fails to explicitly teach backplanes. However, it is well known in the art for cards/modules to connect to backplanes.

Therefore, it would have been obvious to one skilled in the art to include backplanes, in order to provide a means for connecting the cards.

3. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kastenholz et al. (US 2006/0007946) in view of Gorshe et al. (US 6,667,973).

Regarding claim 74, Kastenholz teaches a switched network card coupled to both the first interface card and the second interface card, but fails to disclose a second switched network card coupled to both the first interface card and the second interface card.

However, Gorshe teaches a second switched network card (Figs. 1b and 4b, HSU located in main shelf 102) coupled to both the first interface card (Fig. 4b, AMU in shelf 404) and the second interface card (AMU in shelf 406).

In view of this, it would have been obvious to one skilled in the art to modify Kastenholz's system by including a second switched network card, in order to provide a back-up switched network card for interconnecting the interface cards.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda Murphy whose telephone number is (571) 272-3185. The examiner can normally be reached on Monday - Friday 9:00 - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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Rhonda Murphy
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RM

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